

INTERNATIONAL
STANDARD

ISO/IEC
13213

ANSI/IEEE
Std 1212

First edition
1994-10-05

**Information technology –
Microprocessor systems – Control
and Status Registers (CSR) Architecture
for microcomputer buses**

*Technologies de l'information –
Systèmes à microprocesseurs – Architecture
des registres de commande et d'état
pour bus de micro-ordinateur*



Reference number
ISO/IEC 13213: 1994(E)
ANSI/IEEE
Std 1212, 1994 Edition

Abstract: The document structure and notation are described, and the objectives and scope of the CSR Architecture are outlined. Transition set requirements, node addressing, node architectures, unit architectures, and CSR definitions are set forth. The ROM specification and bus standard requirements are covered.

Keywords: CSR Architecture, bus architecture, bus standard, interoperability, microprocessors, node addressing, registers, transaction sets

The Institute of Electrical and Electronics Engineers, Inc.
345 East 47th Street, New York, NY 10017-2394, USA

Copyright © 1994 by the Institute of Electrical and Electronics Engineers, Inc.
All rights reserved. Published 1994. Printed in the United States of America

ISBN 1-55937-448-9

No part of this publication may be reproduced in any form, in an electronic retrieval system or otherwise, without the prior written permission of the publisher.

October 5, 1994

SH94220

ISO/IEC 13213 : 1994
[ANSI/IEEE Std 1212, 1994 Edition]
(Incorporates ANSI/IEEE Std 1212-1991)

Information technology— Microprocessor systems—Control and Status Registers (CSR) Architecture for microcomputer buses

Sponsor

**Microprocessor and Microcomputer Standards Committee
of the
IEEE Computer Society**



Adopted as an International Standard by the
International Organization for Standardization
and by the
International Electrotechnical Commission



Published by
The Institute of Electrical and Electronics Engineers, Inc.



Foreword

ISO (the International Organization for Standardization) and IEC (the International Electrotechnical Commission) form the specialized system for worldwide standardization. National bodies that are member of ISO or IEC participate in the development of International Standards through technical committees established by the respective organization to deal with particular fields of technical activity. ISO and IEC technical committees collaborate in fields of mutual interest. Other international organizations, governmental and nongovernmental, in liaison with ISO and IEC, also take part in the work.

In the field of information technology, ISO and IEC have established a joint technical committee, ISO/IEC JTC1 1. Draft International Standards adopted by the joint technical committee are circulated to national bodies for voting. Publication as an International Standard requires approval by at least 75% of the national bodies casting a vote.

In 1994, ANSI/IEEE Std 1212-1991 was adopted by ISO/IEC JTC1, as draft International Standard ISO/IEC DIS 13213. This edition incorporates editorial comments received in the review of ISO/IEC DIS 13213.



International Organization for Standardization/International Electrotechnical Commission
Case postale 56 • CH-1211 Genève 20 • Switzerland

IEEE Standards documents are developed within the Technical Committees of the IEEE Societies and the Standards Coordinating Committees of the IEEE Standards Board. Members of the committees serve voluntarily and without compensation. They are not necessarily members of the Institute. The standards developed within IEEE represent a consensus of the broad expertise on the subject within the Institute as well as those activities outside of IEEE that have expressed an interest in participating in the development of the standard.

Use of an IEEE Standard is wholly voluntary. The existence of an IEEE Standard does not imply that there are no other ways to produce, test, measure, purchase, market, or provide other goods and services related to the scope of the IEEE Standard. Furthermore, the viewpoint expressed at the time a standard is approved and issued is subject to change brought about through developments in the state of the art and comments received from users of the standard. Every IEEE Standard is subjected to review at least every five years for revision or reaffirmation. When a document is more than five years old and has not been reaffirmed, it is reasonable to conclude that its contents, although still of some value, do not wholly reflect the present state of the art. Users are cautioned to check to determine that they have the latest edition of any IEEE Standard.

Comments for revision of IEEE Standards are welcome from any interested party, regardless of membership affiliation with IEEE. Suggestions for changes in documents should be in the form of a proposed change of text, together with appropriate supporting comments.

Interpretations: Occasionally questions may arise regarding the meaning of portions of standards as they relate to specific applications. When the need for interpretations is brought to the attention of IEEE, the Institute will initiate action to prepare appropriate responses. Since IEEE Standards represent a consensus of all concerned interests, it is important to ensure that any interpretation has also received the concurrence of a balance of interests. For this reason IEEE and the members of its technical committees are not able to provide an instant response to interpretation requests except in those cases where the matter has previously received formal consideration.

Comments on standards and requests for interpretations should be addressed to:

Secretary, IEEE Standards Board
445 Hoes Lane
P.O. Box 1331
Piscataway, NJ 08855-1331
USA

IEEE Standards documents may involve the use of patented technology. Their approval by the Institute of Electrical and Electronics Engineers does not mean that using such technology for the purpose of conforming to such standards is authorized by the patent owner. It is the obligation of the user of such technology to obtain all necessary permissions.

Introduction

(This introduction is not a part of this International Standard or of ANSI/IEEE Std 1212, 1994 Edition.)

Bus standards have often been set by hardware designers who have focused on the transport mechanisms for sending read and write transactions on a bus. Additional software considerations are needed to ensure interoperability between boards, as users of current bus “standards” have discovered. Therefore, many bus standards have been supplemented with one or several *de facto* or recommended register architectures, which have usually differed for each bus standard.

Through the cooperative efforts of the P1394 Serial Bus, P896 Futurebus+, and P1596 Scalable Coherent Interface (SCI) Working Groups, the need for a more formal approach to defining a common scalable bus-technology-independent Control and Status Register (CSR) Architecture was recognized. The hope is that, by sharing a uniform CSR Architecture, these systems will minimize the software and firmware changes when migrating a processor from one system bus to another or when bridging from one bus to another, and that software costs for migrating between standards (as technology evolves) will be reduced. The P1212 CSR Architecture Working Group was fortunate to have the wide range of bus technologies (from approximately 40 Mb/s for Serial Bus to approximately 1 Gbyte/s for SCI) to test the performance and cost scalability of its designs. The popularity of the Futurebus+ standard ensured that the CSR Architecture specification would be reviewed by a large audience for use in a wide variety of applications.

The scope of the CSR Architecture includes the definition of the generic registers needed to initialize, configure, and test nodes within a system. Other broadcast registers are sufficiently standardized to ensure interoperability between modules supplied by different vendors. The CSR document also defines address-space maps, bus transaction sets (reads, writes, and locks), and ROM data formats.

Protocols are defined for interrupting processors, passing messages, and for accurately synchronizing distributed clocks. These definitions are intended to provide a sufficient and standard framework for the design of vendor-dependent unit architectures. Parts of this CSR Architecture are likely to indirectly influence the processor designs of the future.

The following is a list of participants in the IEEE Control and Status Register (CSR) Working Group at the time ANSI/IEEE Std 1212-1991 was approved:

David V. James, *Chair*

Barbara Aichinger	Tony Grigg	Mira Pauker
Knut Alnes	David B. Gustavson	Chet Pawlowski
Robert S. Baxter	Claes-Göran Gustavsson	James M. Pexa
Harrison Beasley	Mark Hassel	Mike Roby
David Brash	David Hawley	Tim Scott
Mark Bunker	Hubert Holierhoek	Don Senzig
Robert C. Carpenter	Ed Jacques	Patricia Smith
D. Del Corso	Marit Jenssen	Joanne Spiller
Jon Crowell	Ernst Kristiansen	Bob Squirrell
Stephen Deiss	Ralph Lachenmaier	Haruhisa Suzuki
Ian Dobson	Jim Leahy	Michael Teener
Emer Dooley	Jim McGrath	John Theus
Michael A. Dorsett	Thanos Mentzelopoulous	Yoshiaki Wakimura
Sam Duncan	Jim Moidel	Mike Wenzel
W.P. Evertz	Klaus Mueller	Martin Whittaker
Frank Fidducia	George Nacht	Hans Wiggers
John R. Fortier	Mitsunori Nakata	Dwight Wilcox
Ralph Frangioso	Richard Napolitano	Mark Williams
	Daniel C. O'Connor	David L. Wright

The following persons were on the balloting committee that approved this document for submission to the IEEE Standards Board:

John Allen	David B. Gustavson	Daniel C. O'Connor
Knut Alnes	Zoltan R. Hunor	Mira Pauker
Harrison A. Beasley	John Hyde	Donald Pavlovich
Kyle M. Black	Ed Jacques	Richard Rawson
John Black	David V. James	Carl Schmiedekamp
Kim Clohessy	Kenneth Jansen	Don Senzig
Jonathan C. Crowell	Hubert Kirrmann	Paul Sweazey
Stephen L. Diamond	Ernst H. Kristiansen	Michael G. Thompson
Samuel Duncan	Gerry Laws	Eike Waltz
Wayne Fischer	James D. Mooney	Hans A. Wiggers
Joseph D. George	Klaus Dieter Mueller	Mark Williams
Andy Glew	Gary A. Nelson	Oren Yuen
	J. D. Nicoud	

When the IEEE Standards Board approved this standard on December 5, 1991, it had the following membership:

Marco W. Migliaro, *Chair*

Donald C. Loughry, *Vice Chair*

Andrew G. Salem, *Secretary*

Dennis Bodson	Thomas L. Hannan	John E. May, Jr.
Paul L. Borrill	Donald N. Heirman	Lawrence V. McCall
Clyde Camp	Kenneth D. Hendrix	Donald T. Michael*
James M. Daly	John W. Horch	Stig L. Nilsson
Donald C. Fleckenstein	Ben C. Johnson	John L. Rankine
Jay Forster*	Ivor N. Knight	Ronald H. Reimer
David F. Franklin	Joseph L. Koepfinger*	Gary S. Robinson
Ingrid Fromm	Irving Kolodny	Terrance R. Whittemore
	Michael A. Lawler	

*Member Emeritus

Also included are the following nonvoting IEEE Standards Board liaisons:

Fernando Aldana
Satish K. Aggarwal
James Beall
Richard B. Engelman
Stanley Warshaw

IEEE Std 1212-1991 was approved by the American National Standards Institute on May 14, 1992.

This page intentionally left blank

Contents

CLAUSE	PAGE
1. Document structure and notation	1
1.1 Document structure	1
1.2 References	1
1.3 Conformance levels	1
1.4 Technical glossary	2
1.5 Bit, byte, and quadlet ordering	9
1.6 Numerical values	9
1.7 C code notation	10
1.8 CSR, ROM, and field notation	10
1.9 Register specification format	11
1.10 Reserved registers and fields	12
2. Objectives and scope	15
2.1 Scope	15
2.2 Objectives	15
3. Transaction set requirements	17
3.1 Transaction overview	17
3.2 Read and write transactions	17
3.3 Noncoherent lock transactions	18
3.4 Transaction errors	20
3.5 Immediate effects	21
4. Node addressing	23
4.1 Node addresses	23
4.2 Extended addressing	23
4.3 64-bit fixed addressing	25
4.4 Private addresses	26
4.5 Initial node space	26
4.6 Extended address spaces	27
4.7 Indirect space	28
4.8 Address space offsets	29
5. Node architectures	31
5.1 Modules, nodes, and units	31
5.2 Node states	32
5.3 Node testing	33
5.3.1 Access-path tests	33
5.3.2 Reset test	33
5.3.3 Diagnostic tests	34
5.3.4 Non-standard diagnostic tests	35
5.4 Multinode modules	36
5.5 On-line replacement (OLR)	36
6. Unit architectures	39

CLAUSE	PAGE
6.1 Unit architecture overview.....	39
6.2 Interrupts.....	39
6.2.1 Interrupt-target registers.....	39
6.2.2 Interrupt-poll registers.....	40
6.3 Message passing.....	41
6.4 Globally synchronized clocks.....	41
6.4.1 Clock overview.....	41
6.4.2 Clock synchronization.....	42
6.4.3 Clock update models.....	43
6.4.4 Updating clock registers.....	44
6.4.5 Clock accuracy requirements.....	45
6.5 Memory unit architectures.....	45
6.6 Unit architecture environment.....	45
7. CSR definitions.....	47
7.1 Register names and offsets.....	47
7.2 Minimal implementations.....	50
7.3 Unsupported register accesses.....	51
7.4 Register definitions.....	51
7.4.1 STATE_CLEAR.....	51
7.4.2 STATE_SET.....	54
7.4.3 NODE_IDS.....	55
7.4.4 RESET_START.....	56
7.4.5 INDIRECT_ADDRESS.....	57
7.4.6 INDIRECT_DATA.....	58
7.4.7 SPLIT_TIMEOUT.....	58
7.4.8 ARGUMENT.....	59
7.4.9 TEST_START.....	61
7.4.10 TEST_STATUS.....	64
7.4.11 UNITS_BASE.....	66
7.4.12 UNITS_BOUND.....	68
7.4.13 MEMORY_BASE.....	69
7.4.14 MEMORY_BOUND.....	70
7.4.15 INTERRUPT_TARGET.....	71
7.4.16 INTERRUPT_MASK.....	72
7.4.17 CLOCK_VALUE.....	72
7.4.18 CLOCK_TICK_PERIOD.....	74
7.4.19 CLOCK_STROBE_ARRIVED.....	75
7.4.20 CLOCK_STROBE_INFO.....	76
7.4.21 Message targets.....	76
7.4.22 ERROR_LOG registers.....	77
8. ROM specification.....	79
8.1 Introduction.....	79
8.1.1 ROM design assumptions.....	79
8.1.2 ROM formats.....	79
8.1.3 Driver and diagnostic identifiers.....	79
8.1.4 ASCII text.....	81
8.1.5 CRC calculations.....	81
8.2 ROM formats.....	83

CLAUSE	PAGE
8.2.1	First ROM quadlet 83
8.2.2	Minimal ROM format 83
8.2.3	General ROM format 83
8.2.4	Directory formats 84
8.2.5	Leaf format..... 86
8.2.6	Textual_descriptor 86
8.3	bus_info_block..... 88
8.4	Root directory entries..... 89
8.4.1	Bus_Dependent_Info 90
8.4.2	Module_Vendor_Id 90
8.4.3	Module_Hw_Version..... 90
8.4.4	Module_Spec_Id 91
8.4.5	Module_Sw_Version 91
8.4.6	Module_Dependent_Info 91
8.4.7	Node_Vendor_Id..... 91
8.4.8	Node_Hw_Version..... 91
8.4.9	Node_Spec_Id 91
8.4.10	Node_Sw_Version 92
8.4.11	Node_Capabilities 92
8.4.12	Node_Unique_Id..... 92
8.4.13	Node_Units_Extent..... 92
8.4.13.1	Node_Units_Extent immediate format..... 93
8.4.13.2	Node_Units_Extent offset format..... 94
8.4.14	Node_Memory_Extent..... 95
8.4.14.1	Node_Memory_Extent immediate format..... 95
8.4.14.2	Node_Memory_Extent offset format 96
8.4.15	Node_Dependent_Info 96
8.4.16	Unit_Directory 96
8.5	Unit directories..... 96
8.5.1	Unit_Spec_Id 97
8.5.2	Unit_Sw_Version..... 97
8.5.3	Unit_Dependent_Info..... 97
8.5.4	Unit_Location 97
8.5.5	Unit_Poll_Mask 98
8.6	Key definitions..... 98
8.7	company_ids 99
8.7.1	company_id assignments 99
8.7.2	company_id mappings 100
9.	Bus standard requirements..... 101

ANNEXES

A.	Bibliography (Informative)..... 103
B.	Bus topologies (Informative)..... 105
B.1	Specialized buses 105
B.1.1	Multiple-bus topologies 105
B.1.2	Dual-port nodes..... 106
B.2	Fault retry protocols..... 106

ANNEXES	PAGE
B.2.1 Hardware fault recovery.....	106
B.2.2 Software fault recovery.....	107
C. System initialization (Informative).....	109
C.1 System initialization summary.....	109
C.2 Node address assignments.....	109
C.3 Processor-cache model.....	110
C.4 Address protection.....	110
C.5 Power distribution models.....	111
D. Bus transactions (Informative).....	113
D.1 Transaction overview.....	113
D.2 Transaction components.....	113
D.3 Request subaction fields.....	113
D.4 Response subaction fields.....	114
E. Bus bridges (Informative).....	117
E.1 Address-invariant mappings.....	117
E.2 Transaction forwarding.....	118
E.3 Transaction ordering.....	119
E.3.1 Split-response transaction ordering.....	119
E.3.2 Buffered-write transparency.....	119
E.3.3 Weakly ordered move transactions.....	120
E.3.4 Queue-dependency deadlocks.....	121
E.4 Address domains.....	122
E.5 Protection boundaries.....	124
E.6 Coherence domains.....	124

Information technology—Microprocessor systems—Control and Status Registers (CSR) Architecture for microcomputer buses

1. Document structure and notation

1.1 Document structure

This International Standard defines the address-space maps, the bus transaction sets, and the node's CSRs. The intention is to provide a sufficient and standard framework for the design of vendor-dependent unit architectures.

The specification includes the format and content of the configuration ROM on the node. The configuration ROM provide the parameters necessary to autoconfigure systems with nonprocessor nodes provided by multiple vendors.

Note that a monarch selection process, which selects one processor to boot the system, is not defined. A monarch selection process would be necessary to initialize a system containing processors provided by different vendors.

The annexes provide background for understanding the usage of this CSR Architecture specification. The CSR Architecture provides the specification upon which conforming designs should be based. The annex clauses illustrate ways that these capabilities could be used. Note that the annexes are nonbinding.

1.2 References

The following standards contain provisions which, through reference in this text, constitute provisions of this International Standard. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this International Standard are encouraged to investigate the possibility of applying the most recent editions of the standards indicated below. Members of IEC and ISO maintain registers of currently valid International Standards.

ANSI/ISO/IEC 9899:1990, Programming Languages—C.^{1,2}

ISO/IEC 646:1991, Information technology—ISO 7-bit coded character set for information interchange.²

¹ Replaces ANSI X3.159-1989.

² ISO documents are available from ISO Central Secretariat, 1 rue de Varembé, Case Postale 56, CH-1211, Genève 20, Switzerland/Suisse; and from the Sales Department, American National Standards Institute, 11 West 42nd Street, 13th Floor, New York, NY 10036-8002, USA.